CLAIMS

What is claimed is:

1. A method, including:

selecting a memory access group size of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from a number B of banks, wherein N is associated with the protocol type, and wherein N is selected so that 2^N is less than or equal to about B so that a plurality of logical addresses associated with the 2^N memory banks is mapped to a plurality of physical addresses associated with the number B of banks.

2. The method of claim 1, wherein the protocol type includes at least a first operation type different from a second operation type.

3. The method of claim 2, wherein the first operation type includes a single-instruction multiple-data operation type, and wherein the second operation type includes a multiple-instruction multiple-data operation type.

4. The method of claim 1, further including:

selecting a first group size for a first data processing unit different than a second group size selected for a second data processing unit, wherein the first data processing unit and the second data processing unit are capable of addressing the number B of banks.

5. The method of claim 1, wherein the indication of a protocol type is selected from one of a hardware indication and a software indication.

6. The method of claim 1, wherein the memory access group size is associated with a selected number of access bits.

7. The method of claim 1, further including:

configuring a crossbar to operate using the memory access group size responsive to receiving the indication of the change in the protocol type.

8. An article including a machine-accessible medium having associated information, wherein the information, when accessed, results in a machine performing:

selecting a memory access group size of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from a number B of banks, wherein N is associated with the protocol type, and wherein N is selected so that 2^N is less than or equal to about B so that a plurality of logical addresses associated with the 2^N memory banks is mapped to a plurality of physical addresses associated with the number B of banks.

9. The article of claim 8, wherein the protocol type is selected from at least one of a single-instruction multiple-data operation type, a multiple-instruction multiple-data operation type, and a combination of the single-instruction multiple-data operation type and the multiple-instruction multiple-data operation type.

10. The article of claim 8, wherein the information, when accessed, results in a machine performing:

selecting a first memory access group size for a first data processing unit different than a second memory access group size; and

selecting the second memory access group size for a second data processing unit, wherein the first data processing unit and the second data processing unit are capable of addressing the number B of banks.

11. An apparatus, including:

a selection module to select a memory access group size for at least one data processing unit of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from a number B of banks, wherein N is associated with the protocol type, and wherein N is selected so that 2^N is less than or equal to about B so that a plurality of logical addresses associated with the 2^N memory banks is mapped to a plurality of physical addresses associated with the number B of banks.

12. The apparatus of claim 11, further including:

a plurality of data processing units including the at least one data processing units, wherein the plurality of data processing units is capable of addressing the number B of banks.

13. The apparatus of claim 12, wherein the plurality of data processing units and the number B of banks are included in a single processing element.

14. The apparatus of claim 12, wherein the memory access group size 2^N is selected from a group of numbers including two raised to a positive integer power, including 2, 4, ..., B.

15. The apparatus of claim 12, further including:

a hardware address generator to generate an address located in the 2^N memory banks.

16. A system, including:

a selection module to select a memory access group size of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from a number B of banks, wherein N is

associated with the protocol type, and wherein N is selected so that 2^N is less than or equal to about B so that a plurality of logical addresses associated with the 2^N memory banks is mapped to a plurality of physical addresses associated with the number B of banks;

a data processing unit capable of addressing the number B of banks; and

an omnidirectional antenna to transmit data processed by the data processing unit.

17. The system of claim 16, further including:

a bus to couple the data processing unit to one of the number B of banks.

18. The system of claim 16, further including:

a memory to store a plurality of memory access group sizes indexed to a corresponding plurality of protocol types.

19. The system of claim 16, further including:

a transceiver to couple a processing element including the data processing unit to the omnidirectional antenna.

20. An apparatus, including:

a number B of memory banks addressable using a memory access group size of about 2^N memory banks responsive to receiving an indication of a change in a protocol type, wherein the group is selected from the number B of banks, wherein N is associated with the protocol type and selected so that 2^N is less than or equal to about B and wherein the protocol type consists of a single-instruction multiple-data operation type, a multiple-instruction multiple-data operation type, and a combination of the single-instruction multiple-data operation type and the multiple-instruction multiple-data operation type.

21. The apparatus of claim 20, wherein the memory access group size is reprogrammable and is selectable in software.

22. The apparatus of claim 20, further including:

a hardware element to store a plurality of output indications based on a corresponding plurality of memory access group sizes and responsive to a corresponding plurality of protocol type indications.

23. A method, including:

controlling a bandwidth of a memory coupled to a plurality of data processing units responsive to a number of data processing units in use so that a plurality of logical addresses associated with the memory is mapped to a plurality of physical addresses associated with the memory.

24. The method of claim 23, wherein the number of data processing units in use is responsive to an indication provided by an application to be executed.

25. The method of claim 23, wherein the bandwidth of the memory is associated with a selected number of access bits provided by the plurality of data processing units.

26. The method of claim 23, wherein controlling the bandwidth further includes:

controlling an address mapping function of the memory.